Please enter the following amendments:

<u>In the Claims</u>:

Claims 1-21 (Canceled)

22.   (Original) A system comprising:

        a communication bus;

        a direct memory access (DMA) device coupled to the

                communication bus, the direct memory access device

                controlling multiple channels of information, each channel

                of the channels of information transferring information

                from a source to a destination in the system via a channel

                transfer; and

        debug control circuitry coupled to the direct memory access

                device, the debug control circuitry selectively providing

                debug messages related to operating parameters of the

                direct memory access device by being programmable on a

                per channel basis.

23.   (Original) The system of claim 22 wherein the operating parameters of the direct memory access device comprise information regarding at least one of whether a transfer boundary occurred and periodic status information.

24.   (Original) The system of claim 22 wherein the debug control circuitry further provides at least one debug message that includes latency information related to system delay of the direct memory access device starting a channel

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transfer after a channel transfer request is received by the direct memory access device.

25.　(Original) A method of real-time debug support in a system comprising

　　　providing a communication bus;

　　　coupling a direct memory access (DMA) device to the

　　　　　communication bus, the direct memory access device

　　　　　controlling channels of information, each channel of the

　　　　　channels of information transferring information from a

　　　　　source to a destination in the system via a channel transfer;

　　　coupling debug control circuitry to the direct memory access

　　　　　device; and

　　　providing debug messages that identify an existence of a DMA

　　　　　channel transfer boundary for at least one predetermined

　　　　　channel of the channels of information.

26.　(Original) The method of claim 25 further comprising:

　　　programming and selecting which of the channels of information

　　　　　controlled by the direct memory access device that the

　　　　　debug messages will identify the existence of channel

　　　　　transfer boundaries.

27.　(Original) The method of claim 25 further comprising:

　　　using one of the debug messages provided by the debug control

　　　　　circuitry to indicate that a channel transfer has started for

　　　　　the at least one predetermined channel.

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28. (Original) The method of claim 27 further comprising:

    using the one of the debug messages to further indicate a status parameter of the at least one predetermined channel.

29. (Original) The method of claim 28 further comprising:

    using the status parameter to indicate one of channel priority of the at least one predetermined channel, a utilization factor of the at least one predetermined channel, and whether a transfer error has previously occurred in connection with the at least one predetermined channel.

30. (Original) The method of claim 27 further comprising:

    using the one of the debug messages to further indicate a time latency associated with the channel transfer indicating system delay between the direct memory access device receiving a request to begin transferring information and actually transferring the information.

31. (Original) The method of claim 25 further comprising:

    using the one of the debug messages provided by the debug control circuitry to indicate that a channel transfer has ended for the at least one predetermined channel.

32. (Original) The method of claim 25 further comprising:

    using the one of the debug messages provided by the debug control circuitry to indicate that each of a plurality of

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minor loop iterations of the at least one predetermined

channel has started.

33.   (Original) The method of claim 25 further comprising:

using the one of the debug messages provided by the debug

control circuitry to indicate that each of a plurality of

minor loop iterations of the at least one predetermined

channel has ended.

34.   (Original) The method of claim 25 further comprising:

using the one of the debug messages provided by the debug

control circuitry to periodically indicate a predetermined

status parameter of the at least one predetermined channel.

35.   (Original) The method of claim 25 further comprising:

providing a plurality of system units, each of the plurality of system

units coupled to the communication bus;

providing a plurality of debug modules for providing the debug

messages, each of the plurality of debug modules being coupled to a

predetermined one of the plurality of system units; and

coupling debug port logic to the plurality of debug modules for

providing the debug messages to a debug port.

Claims 36-45 (Canceled)

46.   (Original) A method of real-time debug support in a system comprising

providing a communication bus;

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coupling a direct memory access (DMA) device to the
communication bus, the direct memory access device
controlling multiple channels of information, each channel
of the channels of information transferring information
from a source to a destination in the system via a channel
transfer; and

coupling debug control circuitry to the direct memory access
device, the debug control circuitry selectively providing
debug messages related to operating parameters of the
direct memory access device by being programmable on a
per channel basis.

47. (Original) The method of claim 46 further comprising implementing the
operating parameters of the direct memory access device as information
regarding at least one of whether a transfer boundary occurred and periodic
status information.

48. (Original) The method of claim 46 further comprising providing at least
one debug message that includes latency information related to system delay
of the direct memory access device starting a channel transfer after a channel
transfer request is received by the direct memory access device.